REMARKS

This Response, filed in reply to the Office Action dated December 12, 2005, is believed to be fully responsive to each point of rejection raised therein. Accordingly, favorable reconsideration on the merits is respectfully requested.

Claims 1-3, 17, 19, 22-24 and 27-29 remain pending the application. Claims 1-3, 17, 19, 22-24 and 27-29 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Yanagita et al. (U.S.P. 5,982,953). Applicant respectfully submits the following arguments in traversal of the prior art rejections.

Applicant's invention relates to a method for image processing which allows display of an originally supplied image without processing delay, while also allowing later viewing, or concurrent viewing of a processed version of the original image. This obviates delays in a preliminary analysis of the original image, for example, while a processed image is generated to assist with analysis. In an exemplary embodiment of the invention, the images are medical images.

Turning to the newly cited art, Yanagita teaches an apparatus for displaying processed and unprocessed images. In relevant part, Fig. 1 illustrates images obtained from an image storage section 1, which are passed via image control section 3 to an image processing section 4. After processing (or passing through) the processing section 5, the image is stored in memory 7 for subsequent display to output 6. In similar regard, in Fig. 13, the processing section 5 precedes the storage of images to respective memories 7a and 7b for displays 6a and 6b.

The Examiner contends that Yanagita teaches each feature of independent claim 1. However, claim 1 describes transferring at least one original image signal to an image output device prior to an operation processing image signal being obtained from a predetermined processing. This sequence is not taught or suggested in Yanagita. This is because the display of information in Yanagita stems from reading of data from local memory 7 (7a, 7b). Col. 7, lines 46-51, which is only provided **after processing** or read through processor 5. Therefore, any processed image displayed must have been processed prior to storage and not subsequent thereto. In the situation where an original image signal it output (such as in display 6a), the processed signal is expressly described as simultaneously displayed (in display 6b). The Examiner concedes this point. Page 3, last 4 lines. Therefore, the order of the transfer to the output device is not expressly required.

Applicant also submits that the image display is controlled via an operator using controls at operation desk (Fig. 13, element 4). The operator may switch between multiple processed images displayed by operation of the display control sections 8a, 8b. This would suggest that the processed images are stored in memories 7a , 7b contemporaneously with any original signals, rather receipt of individual images one at a time for display purposes. This would indicate that the original image is not output prior to the output of processing.

The Examiner concludes that the original image is stored in memory prior to the arrival of the processed image. Applicant submits that Yanagita is silent on this point, and that the switching between different processed images would indicate that the processed images and the original image arrive in the memory in a contemporaneous manner. Even assuming *arguendo*

that the Examiner's statement is true, that the original image is stored in memory prior to arrival of a processed image, the claim describes transfer to an output device prior to the operation processing output. The mere fact that the original may be stored in memory 7 first does not indicate its transfer to an output device (display 6) prior to processing. Because the memory 7 must store data to be displayed, it is more likely that the processed data must be received and processed by processor element 5 before any control activity of the display 6. Any ambiguity in the Yanagita disclosure on this point would not support an anticipation rejection. Therefore, claim 1 is patentable for at least these reasons.

Because independent claim 27 includes recitations analogous to claim 1, claim 27 is also patentable for the above reasons. The remaining claims are patentable based on their dependency.

With further regard to claims 2 and 3, these claims describe locations of operation processing device - such as at the side of the image output device (claim 2) and at the side of the image input apparatus (claim 3). The Examiner cannot consistently maintain that the embodiments of Yanagita teach mutually different positioning. Either the rejection of claim 2 or the rejection of claim 3 should be withdrawn.

Claim 19 makes it clear that output of the image of the original image signal precedes an output from the processor. This is not taught by Yanagita where the order of the outputs is not clearly stated.

With further regard to claim 22, this claim describe the processing of upper and lower surface signals of a phosphor sheet. The Examiner concedes that Yanagita fails to teach this feature. This alone would warrant withdrawal of the anticipation rejection. The Examiner attempts to cure this deficiency with reference to JP 08-336517. However, despite the Examiner's characterization to the contrary, the anticipation rejection is not appropriate in this situation because multiple other types of processing are possible. In other words, there is no inherent requirement that Yanagita must incorporate the nature of processing described by the claims or disclosed by the JP reference. For example, Yanagita serves as its own disclosure for processing, such as addition, subtraction and edge enhancement. Col. 8, lines 28-40. Therefore, claim 22 is patentable for this additional reason. Claim 28 is patentable for the same rationale.

With further regard to claim 23, this claim describes masking. The Examiner cites col.8, lines 30-32 of Yanagita to teach this feature. Col. 8, lines 30-32 describe "preprocessing" as a reduction process, not masking in the manner claimed. Therefore, claim 23 is patentable for this additional reason.

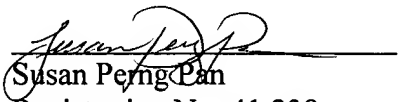
With further regard to claim 29, this claim describes a parallel output of images. The Examiner relies generally on Fig. 13 to teach this feature. However, neither Fig. 13 nor its supporting disclosure teaches a parallel output as claimed.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the

Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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